CLAIMS:

1. Method for testing a testable electronic device having a first plurality of test arrangements and a second plurality of test arrangements, the method comprising the steps of:

serially communicating first test data (102, 106) between a first shift register (110, 150, 210, 250, 410, 450) and a first test data channel (202, 206, 402, 406), and at least partially simultaneous therewith, serially communicating second test data (104, 108) between a second shift register (130, 170, 230, 270, 430, 470) and a second test data channel (204, 208, 404, 408); and

parallelly communicating the first test data (102, 106) between the first plurality of test arrangements and the first shift register (110, 150, 210, 250, 410, 450), and at least partially simultaneous therewith, parallelly communicating the second test data (104, 108) between the second plurality of test arrangements and the second shift register (130, 170, 230, 270, 430, 470).

2. A method as claimed in claim 1, comprising the further steps of copying the first test data (102, 106) from the first shift register (110, 410) into a first buffer register (120, 420) and copying the second test data (104, 108) from the second shift register (130, 430) into a second buffer register (140, 440).

3. A method as claimed in claim 1 or 2, wherein:

the step of serially communicating the first test data (102) is directed from the first test data channel (202, 402) to the first shift register (110, 210, 410);

the step of serially communicating the second test data (104) is directed from the second test data channel (204, 404) to the second shift register (130, 230, 430);

the step of parallelly communicating the first test data (102) is directed from the first shift register (110, 210, 410) to the first plurality of test arrangements; and

the step of parallelly communicating the second test data (104) is directed from the second shift register (130, 230, 430) to the second plurality of test arrangements.

4. A method as claimed in claim 3, comprising the further steps of: parallelly receiving first test result data (106) from the first plurality of test arrangements in a third shift register (150, 250, 450), and at least partially simultaneous therewith, parallelly receiving second test result data (108) from the second plurality of test arrangements in a fourth shift register (170, 270, 470); and

serially submitting the first test result data (106) from the third shift register (150, 250, 450) to a third test data channel (206, 406), and at least partially simultaneous therewith, serially submitting the second test result data (108) from the fourth shift register (170, 270, 470) to a fourth test data channel (208, 408).

5. A testable electronic device (200), comprising:

a first plurality of test arrangements (220) and a second plurality of test arrangements (240);

a first contact (202, 206) and a second contact (204, 208);

a first shift register (210, 250) coupled between the first contact (202, 206) and the first plurality of test arrangements (220) for serially communicating first test data with the first contact (202, 206), and for parallelly communicating the first test data with the first plurality of test arrangements (220); and

a second shift register (230, 270) coupled between the second contact (204, 208) and the second plurality of test arrangements (240) for serially communicating second test data with the second contact (204, 208) at least partially simultaneous with the serial communication of the first test data, and for parallelly communicating the second test data with the second plurality of test arrangements (240) at least partially simultaneous with the parallel communication of the first test data.

6. A testable electronic device (200) as claimed in claim 5, wherein the first shift register (210, 250) is coupled to the second shift register (230, 270).

7. A testable electronic device (200) as claimed in claim 6, wherein the first shift register (210, 250) and the second shift register (230, 270) are part of a boundary scan register (290).

8. A testable electronic device (200) as claimed in claim 5, wherein the first shift register (210) is arranged to communicate the first test data from the first contact (202) to the

first plurality of test arrangements (220), and the second shift register (230) is arranged to communicate the second test data from the second contact (204) to the second plurality of test arrangements (240), and wherein the electronic device (200) further comprises:

a third contact (206) and a fourth contact (208);

a third shift register (250) coupled between the third contact (206) and the first plurality of test arrangements (220) for serially submitting first test result data to the third contact (206), and for parallelly receiving the first test result data from the first plurality of test arrangements (220); and

a fourth shift register (270) coupled between the fourth contact (208) and the second plurality of test arrangements (240) for serially submitting second test result data to the fourth contact (208) at least partially simultaneous with the serial submission of the first test result data, and for parallelly receiving the second test result data from the second plurality of test arrangements (240) at least partially simultaneous with the parallel reception of the first test result data.

9. A testable electronic device (200) as claimed in claim 8, wherein the third shift register (250) is coupled to the fourth shift register (270).

10. A testable electronic device (200) as claimed in claim 9, wherein the third shift register (250) and the fourth shift register (270) are part of a boundary scan register (290).

11. Test apparatus (400) for testing a testable electronic device having a first plurality of test arrangements and a second plurality of test arrangements, the test apparatus (400) comprising:

a first test data channel (402) and a second test data channel (404);

a first shift register (410) coupled to the first test data channel (402) for serially communicating first test data with the first test data channel (402), and for parallelly communicating the first test data with the first plurality of test arrangements; and

a second shift register (430) coupled to the second test data channel (404) for serially communicating second test data with the second test data channel (404) at least partially simultaneous with the serial communication of the first test data, and for parallelly communicating the second test data with the second plurality of test arrangements at least partially simultaneous with the parallel communication of the first test data.

12. A test apparatus (400) as claimed in claim 12, wherein the first shift register (410) is coupled to a first buffer register (420), and the second shift register (430) is coupled to a second buffer register (440).

13. A test apparatus (400) as claimed in claim 13, wherein the first shift register (410) and the second shift register (430) are responsive to a first clock (CLK1) and the first buffer register (420) and the second buffer register (440) are responsive to a second clock (CLK2).

14. A test apparatus (400) as claimed in claim 12, wherein the first shift register (410) is arranged to communicate the first test data from the first test channel (402) to the first plurality of test arrangements, and the second shift register (430) is arranged to communicate the second test data from the second test channel (404) to the second plurality of test arrangements, and wherein the test apparatus (400) further comprises:

a third test channel (406) and a fourth test channel (408);

a third shift register (450) coupled to the third test data channel (406) for serially submitting first test result data to the third test data channel (406), and for parallelly receiving the first test result data from the first plurality of test arrangements; and

a fourth shift register (470) coupled to the fourth data channel (408) for serially submitting second test result data to the fourth test data channel (408) at least partially simultaneous with the serial submission of the first test result data, and for parallelly receiving the second test result data from the second plurality of test arrangements at least partially simultaneous with the parallel reception of the first test result data.

15. A test apparatus (400) as claimed in claim 14, the test apparatus (400) further comprising:

a first plurality of tri-state buffers (480), each tri-state buffer from the first plurality of tri-state buffers (480) coupling an output of the first shift register (410) to an input of the third shift register (450); and

a second plurality of tri-state buffers (490), each tri-state buffer from the second plurality of tri-state buffers (490) coupling an output of the second shift register (430) to an input of the fourth shift register (470).